



AD1672S Data Sheet Revision

Data Sheet Specification Comparison

Rev P

4.0 Electrical Table:

Table I						
Parameter (see notes at end of table)	Symbol	Conditions 1/ Unless Otherwise Specified	Sub Group	Limit Min	Limit Max	Units
Resolution		No Missing Codes	1,2,3	12		Bits
Supply Current	I _{VCC} I _{VDD} I _{DRVDD}		1,2,3		65 2 2	mA
Power Dissipation	PD		1,2,3		363	mW
Power supply rejection 3/	PSR	V _{CC} = 5.0V ± 0.25V V _{DD} = 5.0V ± 0.25V V _{DRVDD} = 3.0V to 5.25V	1,2,3	-0.3 -0.3 -0.1	0.3 0.3 0.1	%FSR
ACCURACY			1,2,3			
Integral Nonlinearity	INL			-2.5	2.5	LSB
Differential Nonlinearity	DNL			-1	1.5	LSB
Offset Zero	VOSE			-0.75	0.75	%FSR
Zero Error 5/				-0.75	0.75	%FSR
Gain Error 2/				-1.5	1.5	%FSR
Internal Voltage Reference 6/	V _O	I _{OUT} = 0.5 mA 4/	1,2,3	2.475	2.525	V

Rev Q

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ACCURACY			1,2,3			
Integral Nonlinearity 7/	INL			-2.5	2.5	LSB
Differential Nonlinearity 7/	DNL			-1	1.5	LSB
Offset Zero	VOSE			-0.75	0.75	%FSR
Zero Error 5/				-0.75	0.75	%FSR
Gain Error 2/				-1.5	1.5	%FSR
Internal Voltage Reference 6/	V _O	I _{OUT} = 0.5 mA 4/	1,2,3	2.475	2.525	V

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Rev P

NOTES:

1/ $V_{CC} = V_{DD} = V_{DRVDD} = +5.0V$.

2/ Includes internal reference error.

3/ Change in full scale as a function of the dc supply voltage.

4/ Current available for external loads. External load should not change during conversion.

5/ Bipolar Mode

6/ The AD1672 includes an onboard +2.5 V reference. The reference input pin (REF IN) can be connected to reference output pin (REF OUT) or a standard external +2.5 V reference can be selected to meet specific system requirements. The reference input voltage can be held with the use of a capacitor. To prevent the AD1672's onboard reference from oscillating when not connected to REF IN, REF OUT must be connected to +5 VVCC. It is possible to connect REF OUT to +5 V due to its output circuit implementation which shuts down the reference

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7/ This parameter is not tested post-irradiation.